FIG. 1

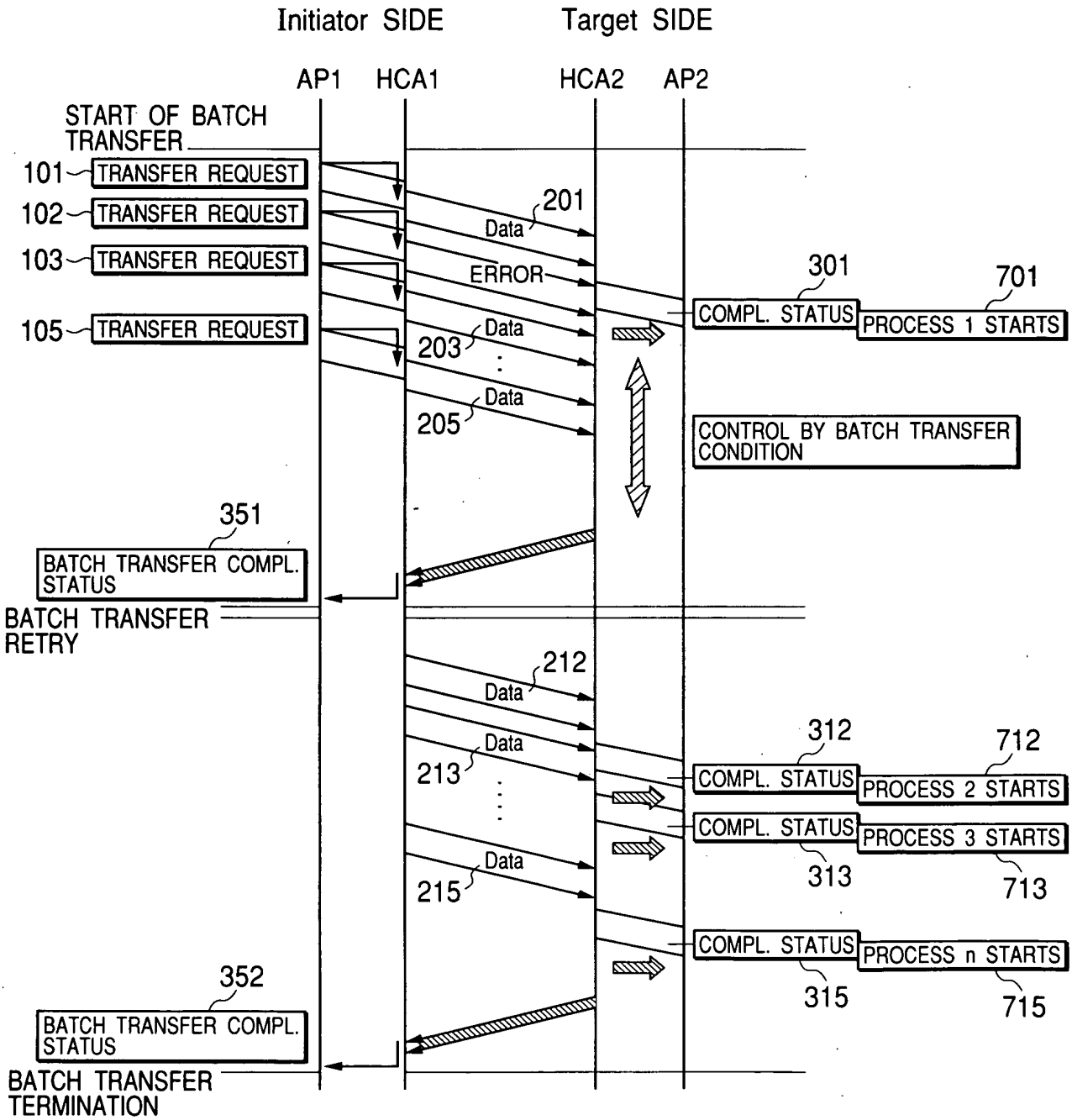
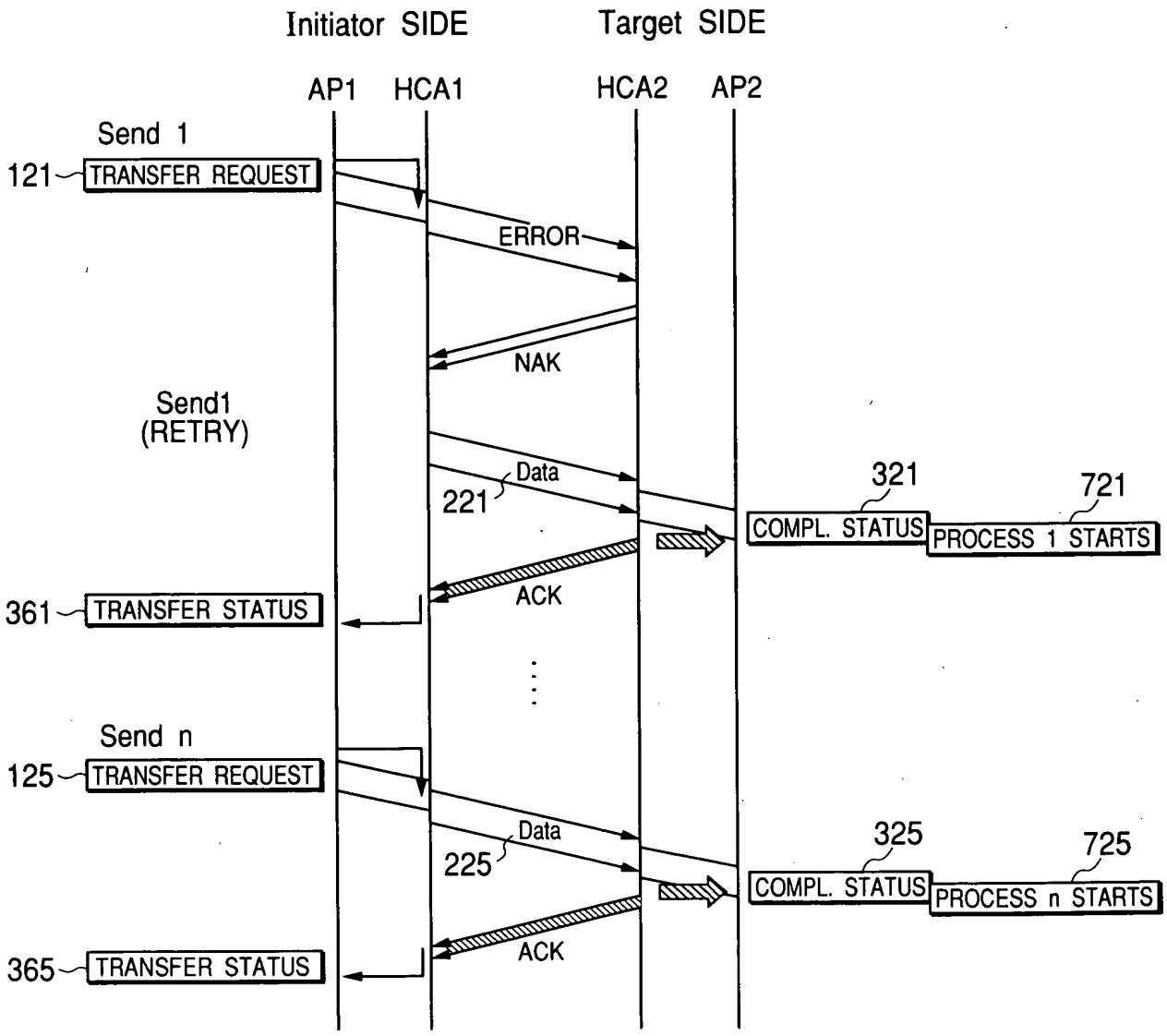

Initiator SIDE
Target SIDE
AP1
HCA1
HCA2
AP2
START OF BATCH TRANSFER
101
TRANSFER REQUEST
102
TRANSFER REQUEST
103
TRANSFER REQUEST
105
TRANSFER REQUEST
201
Data
ERROR
203
Data
205
Data
301
COMPL. STATUS
701
PROCESS 1 STARTS
CONTROL BY BATCH TRANSFER CONDITION
351
BATCH TRANSFER COMPL. STATUS
BATCH TRANSFER RETRY
212
Data
213
Data
215
Data
312
COMPL. STATUS
712
PROCESS 2 STARTS
COMPL. STATUS
PROCESS 3 STARTS
313
713
COMPL. STATUS
PROCESS n STARTS
315
715
352
BATCH TRANSFER COMPL. STATUS
BATCH TRANSFER TERMINATION

FIG. 2



IN A CONVENTIONAL METHOD OF DATA TRANSFER (SINGLE DATA TRANSFER BASE), OVERHEADS OCCUR BEFORE AND AFTER EVERY DATA TRANSFER AND THIS IS A BOTTLENECK OF INCREASING EFFICIENCY OF TRANSFER.

FIG. 3

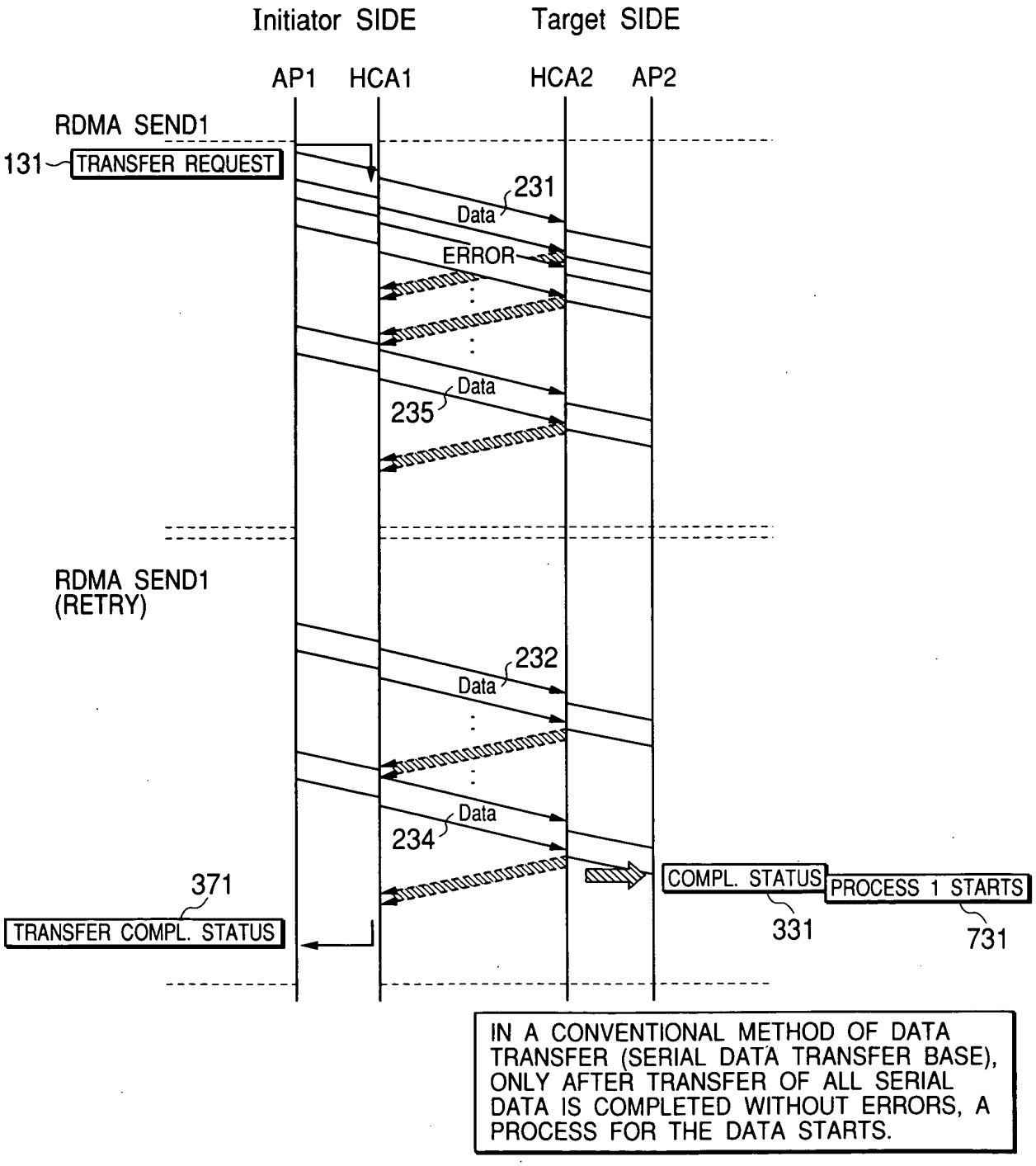

Initiator SIDE
Target SIDE
AP1
HCA1
HCA2
AP2
RDMA SEND1
131
TRANSFER REQUEST
231
Data
ERROR
Data
235
RDMA SEND1
(RETRY)
232
Data
Data
234
371
TRANSFER COMPL. STATUS
COMPL. STATUS
PROCESS 1 STARTS
331
731
IN A CONVENTIONAL METHOD OF DATA TRANSFER (SERIAL DATA TRANSFER BASE), ONLY AFTER TRANSFER OF ALL SERIAL DATA IS COMPLETED WITHOUT ERRORS, A PROCESS FOR THE DATA STARTS.

FIG. 4

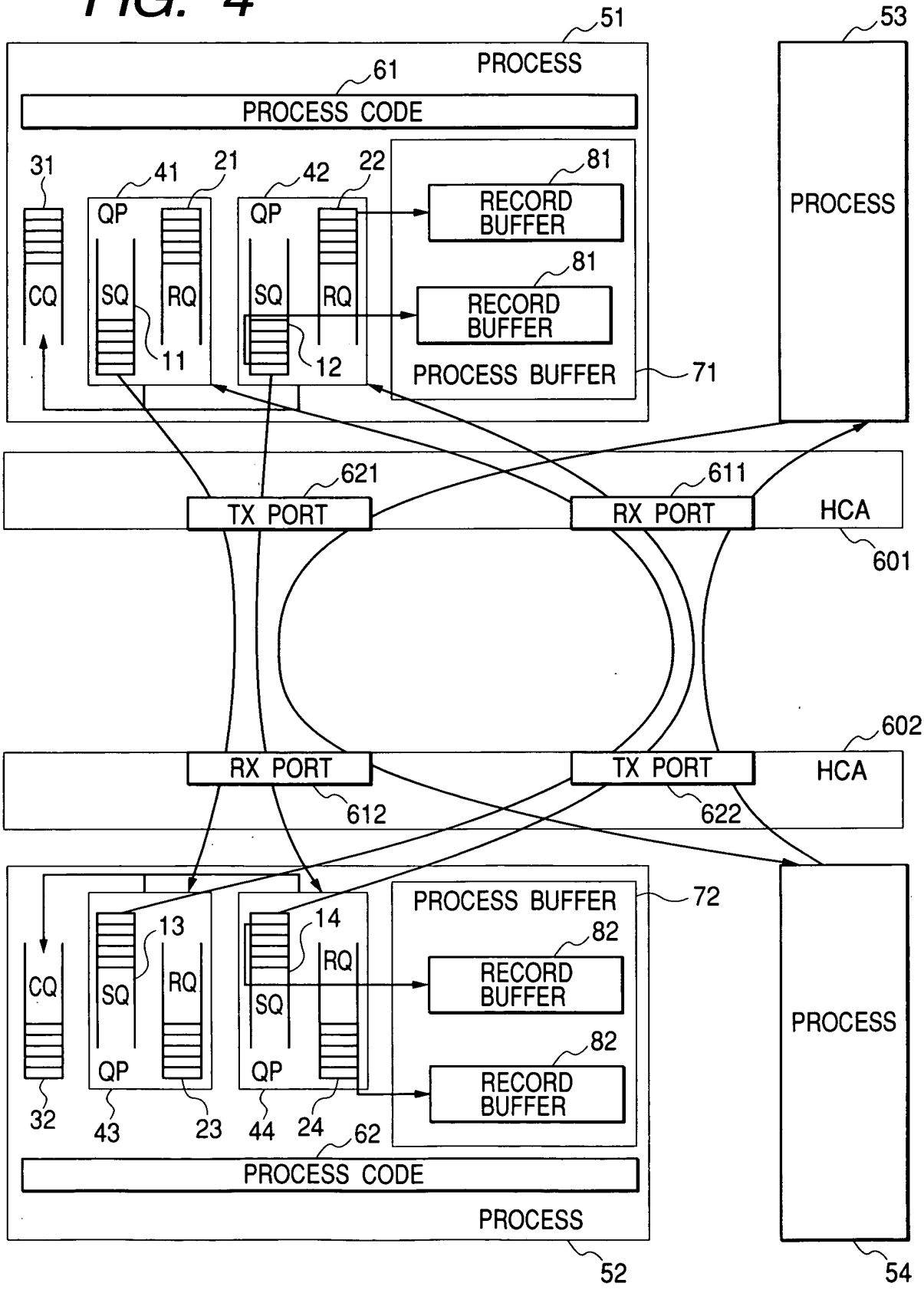

51
PROCESS
61
PROCESS CODE
31
41
21
42
22
81
RECORD BUFFER
QP
SQ
RQ
CQ
11
12
PROCESS BUFFER
71
53
PROCESS
621
611
TX PORT
RX PORT
HCA
601
602
RX PORT
TX PORT
HCA
612
622
PROCESS BUFFER
72
13
14
82
RECORD BUFFER
32
43
23
44
24
62
PROCESS CODE
PROCESS
52
54

FIG. 5

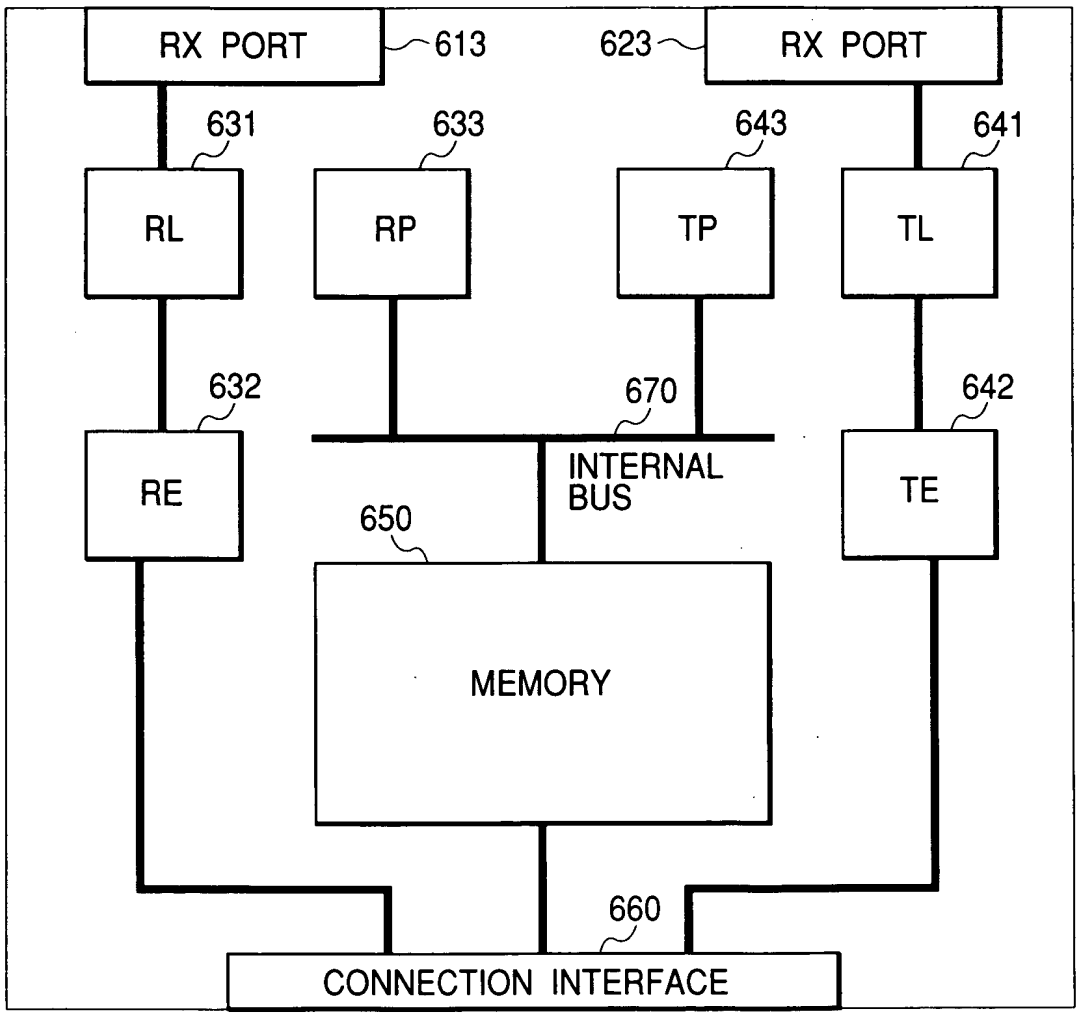

RX PORT
613
623
RX PORT
631
633
643
641
RL
RP
TP
TL
632
670
642
RE
INTERNAL BUS
TE
650
MEMORY
660
CONNECTION INTERFACE

FIG. 6

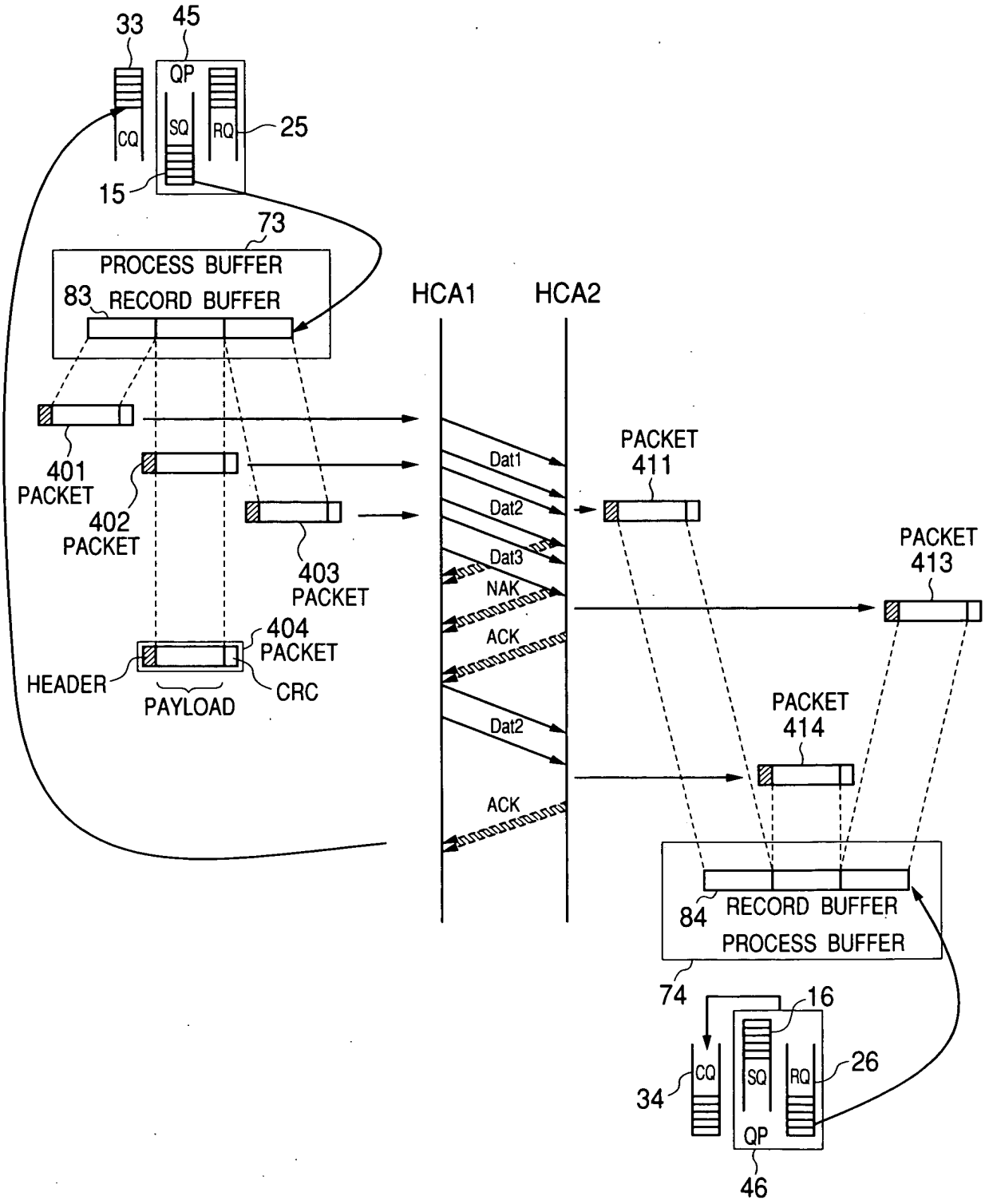

33
45
QP
CQ
SQ
RQ
25
15
73
PROCESS BUFFER
83
RECORD BUFFER
HCA1
HCA2
401
PACKET
402
PACKET
403
PACKET
404
PACKET
HEADER
PAYLOAD
CRC
Dat1
Dat2
Dat3
NAK
ACK
Dat2
ACK
PACKET
411
PACKET
413
PACKET
414
84
RECORD BUFFER
PROCESS BUFFER
74
16
34
CQ
SQ
RQ
26
QP
46

FIG. 7

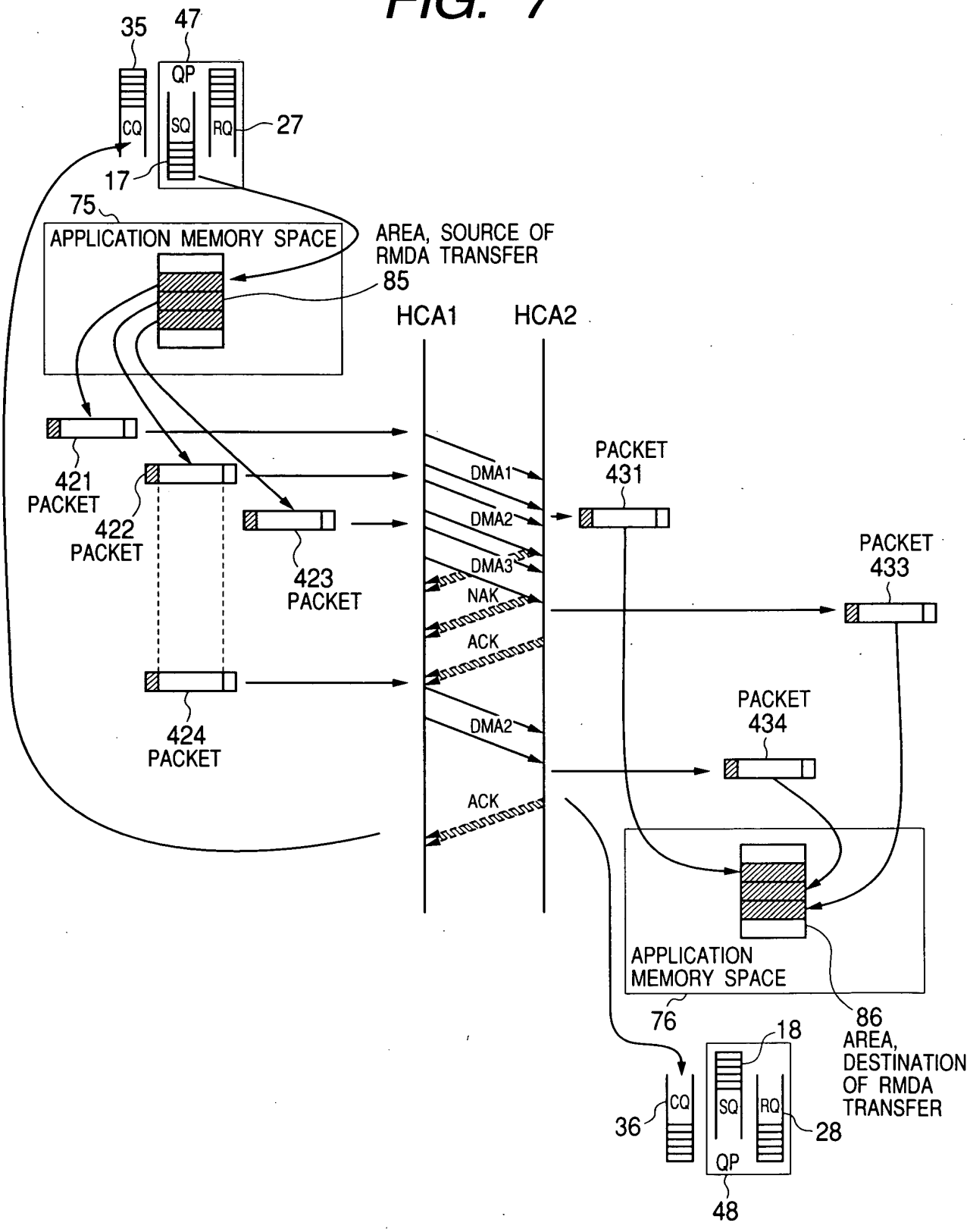

35
47
QP
CQ
SQ
RQ
27
17
75
APPLICATION MEMORY SPACE
AREA, SOURCE OF RMDA TRANSFER
85
HCA1
HCA2
421 PACKET
422 PACKET
423 PACKET
424 PACKET
DMA1
DMA2
DMA3
NAK
ACK
DMA2
ACK
PACKET 431
PACKET 433
PACKET 434
APPLICATION MEMORY SPACE
76
86
AREA, DESTINATION OF RMDA TRANSFER
18
36
CQ
SQ
RQ
28
QP
48

FIG. 8

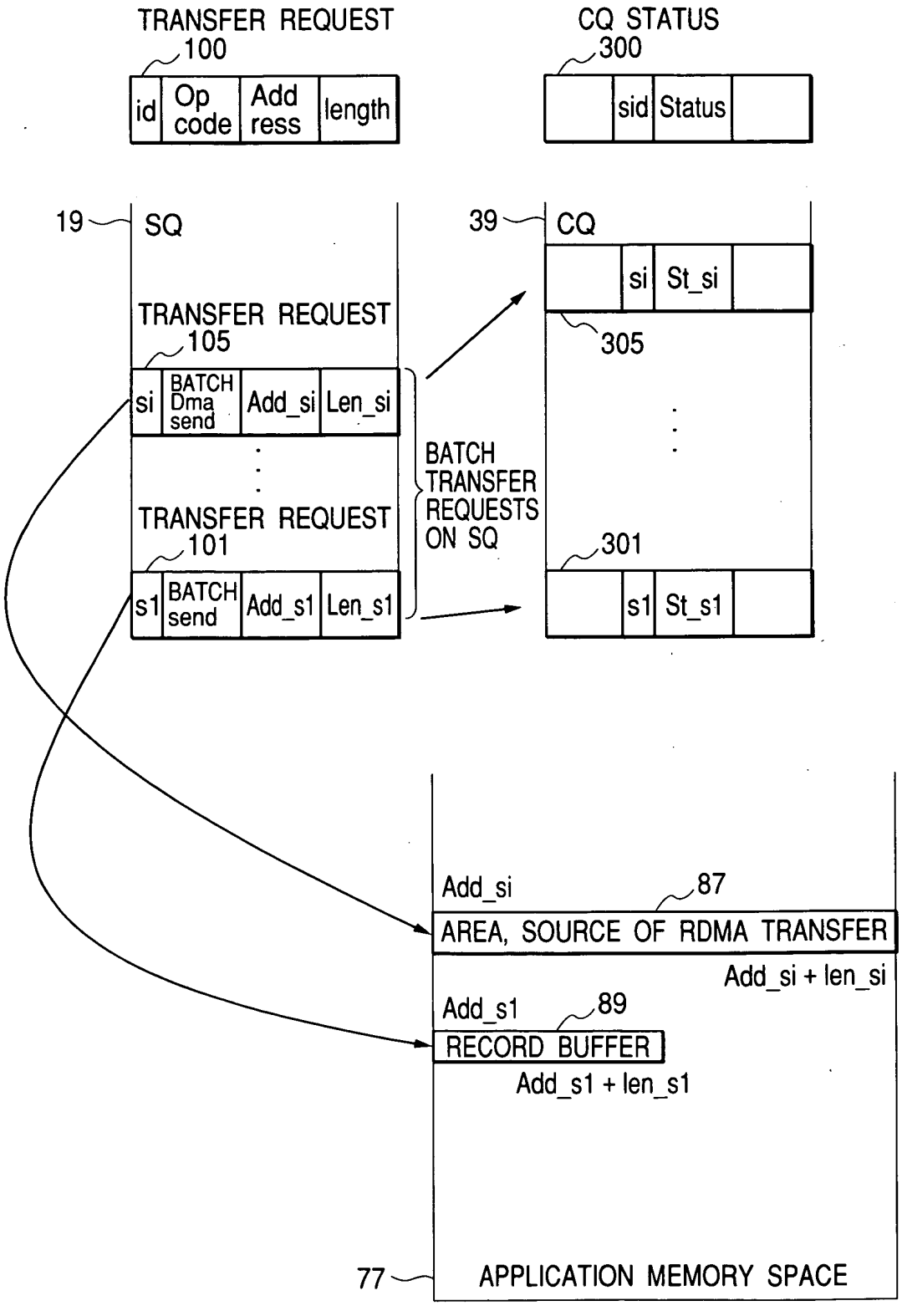

TRANSFER REQUEST
100
id
Op code
Add ress
length
CQ STATUS
300
sid
Status
19
SQ
39
CQ
TRANSFER REQUEST
105
si
BATCH Dma send
Add_si
Len_si
si
St_si
305
TRANSFER REQUEST
101
s1
BATCH send
Add_s1
Len_s1
BATCH TRANSFER REQUESTS ON SQ
301
s1
St_s1
Add_si
87
AREA, SOURCE OF RDMA TRANSFER
Add_si + len_si
Add_s1
89
RECORD BUFFER
Add_s1 + len_s1
77
APPLICATION MEMORY SPACE

FIG. 9

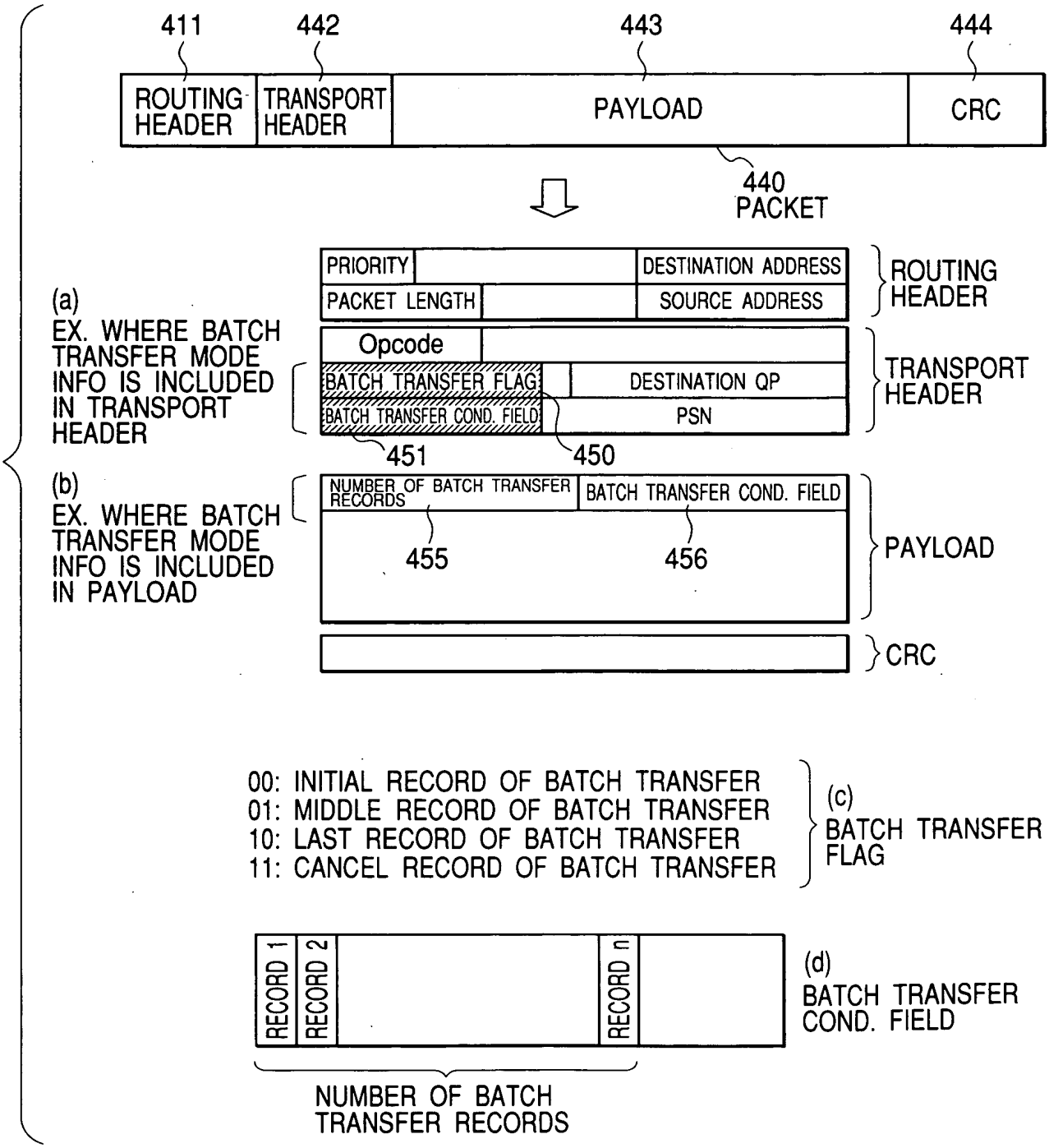

411
442
443
444
ROUTING HEADER
TRANSPORT HEADER
PAYLOAD
CRC
440
PACKET
(a)
EX. WHERE BATCH TRANSFER MODE INFO IS INCLUDED IN TRANSPORT HEADER
PRIORITY
DESTINATION ADDRESS
PACKET LENGTH
SOURCE ADDRESS
ROUTING HEADER
Opcode
BATCH TRANSFER FLAG
DESTINATION QP
BATCH TRANSFER COND. FIELD
PSN
TRANSPORT HEADER
451
450
(b)
EX. WHERE BATCH TRANSFER MODE INFO IS INCLUDED IN PAYLOAD
NUMBER OF BATCH TRANSFER RECORDS
BATCH TRANSFER COND. FIELD
455
456
PAYLOAD
CRC
00: INITIAL RECORD OF BATCH TRANSFER
01: MIDDLE RECORD OF BATCH TRANSFER
10: LAST RECORD OF BATCH TRANSFER
11: CANCEL RECORD OF BATCH TRANSFER
(c)
BATCH TRANSFER FLAG
RECORD 1
RECORD 2
RECORD n
(d)
BATCH TRANSFER COND. FIELD
NUMBER OF BATCH TRANSFER RECORDS

FIG. 10

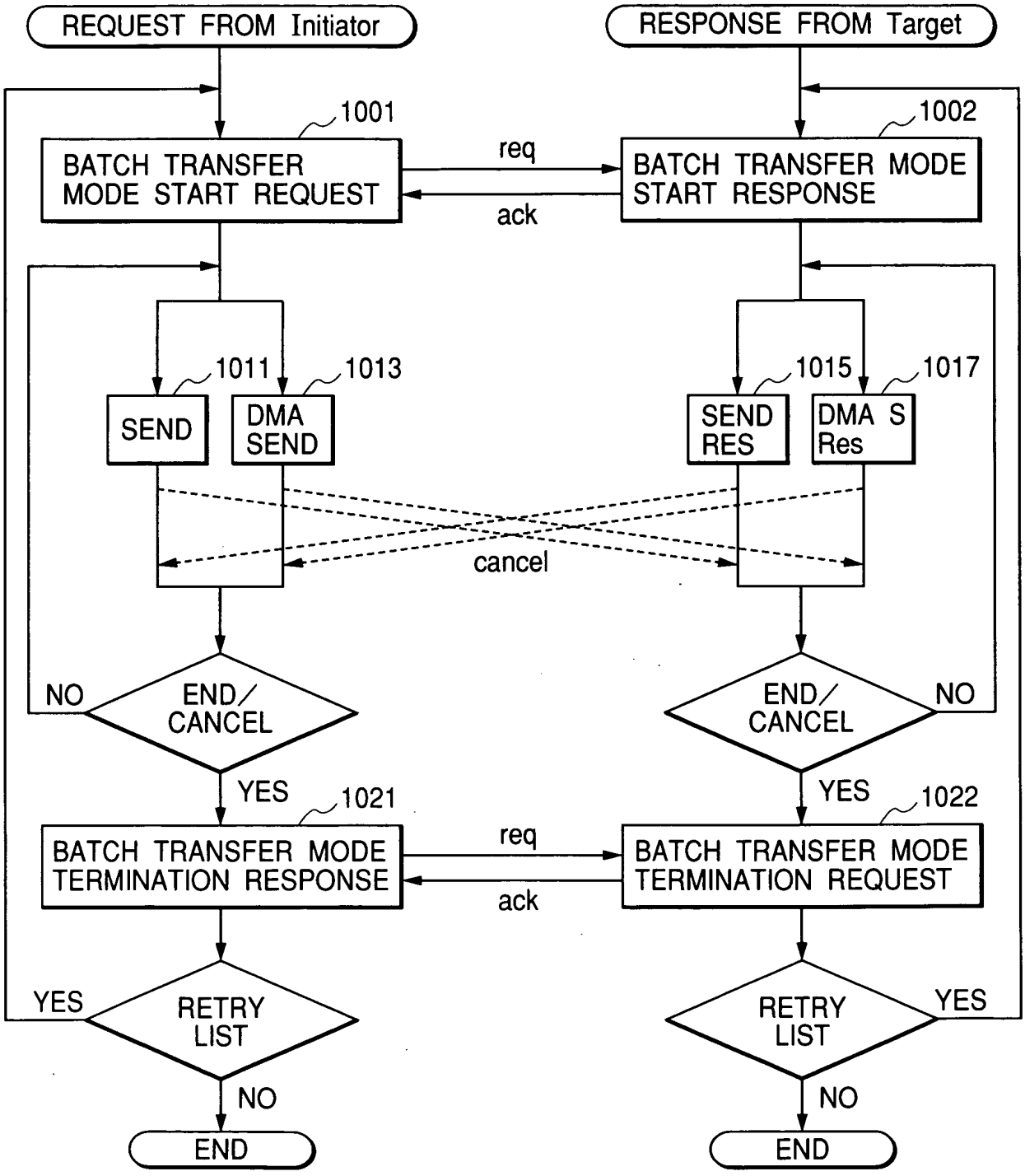

REQUEST FROM Initiator
RESPONSE FROM Target
1001
1002
BATCH TRANSFER MODE START REQUEST
req
ack
BATCH TRANSFER MODE START RESPONSE
1011
1013
1015
1017
SEND
DMA SEND
SEND RES
DMA S Res
cancel
NO
END/ CANCEL
END/ CANCEL
NO
YES
1021
YES
1022
BATCH TRANSFER MODE TERMINATION RESPONSE
req
ack
BATCH TRANSFER MODE TERMINATION REQUEST
YES
RETRY LIST
RETRY LIST
YES
NO
NO
END
END

FIG. 11

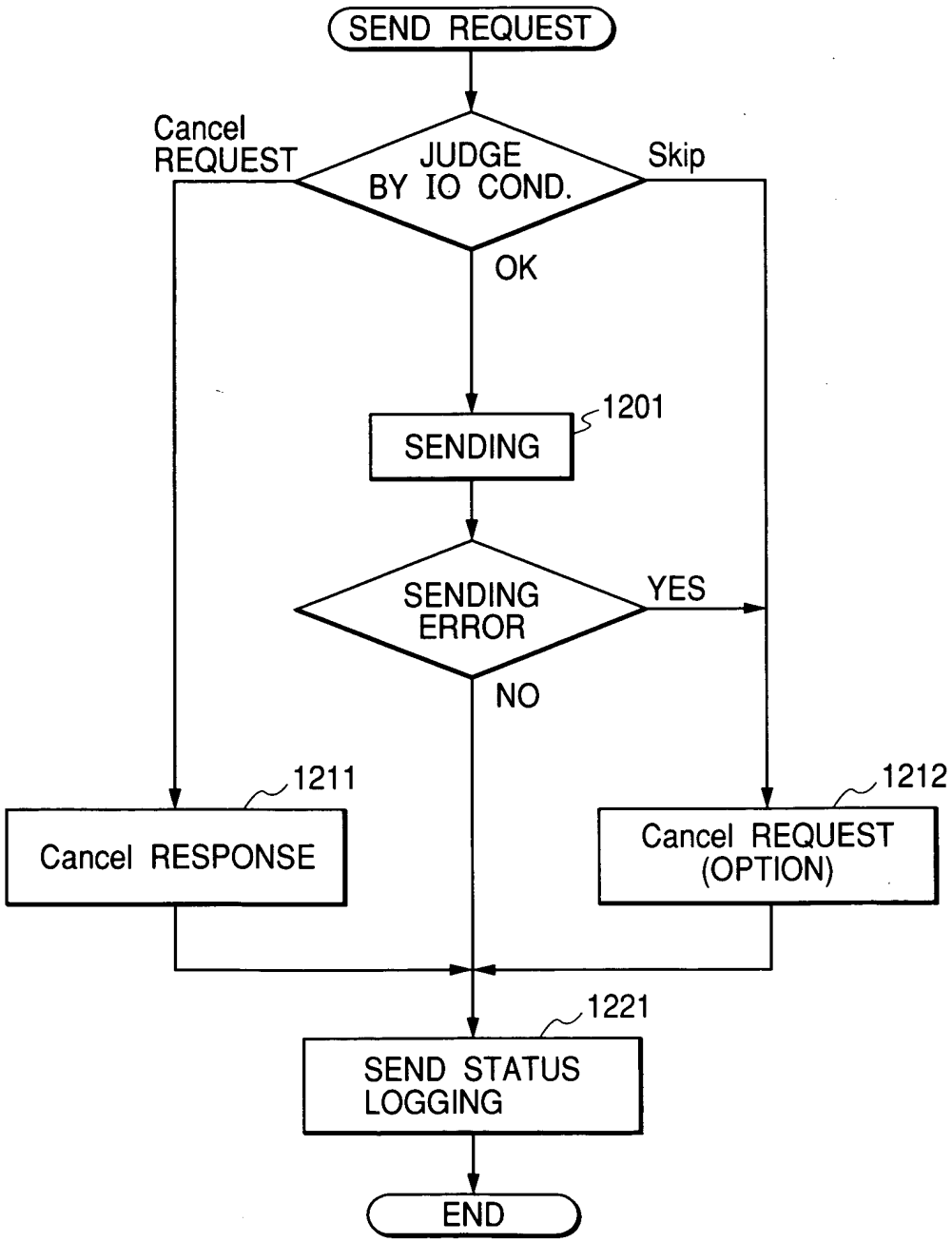

SEND REQUEST
Cancel REQUEST
JUDGE BY IO COND.
Skip
OK
1201
SENDING
SENDING ERROR
YES
NO
1211
Cancel RESPONSE
1212
Cancel REQUEST (OPTION)
1221
SEND STATUS LOGGING
END

FIG. 12

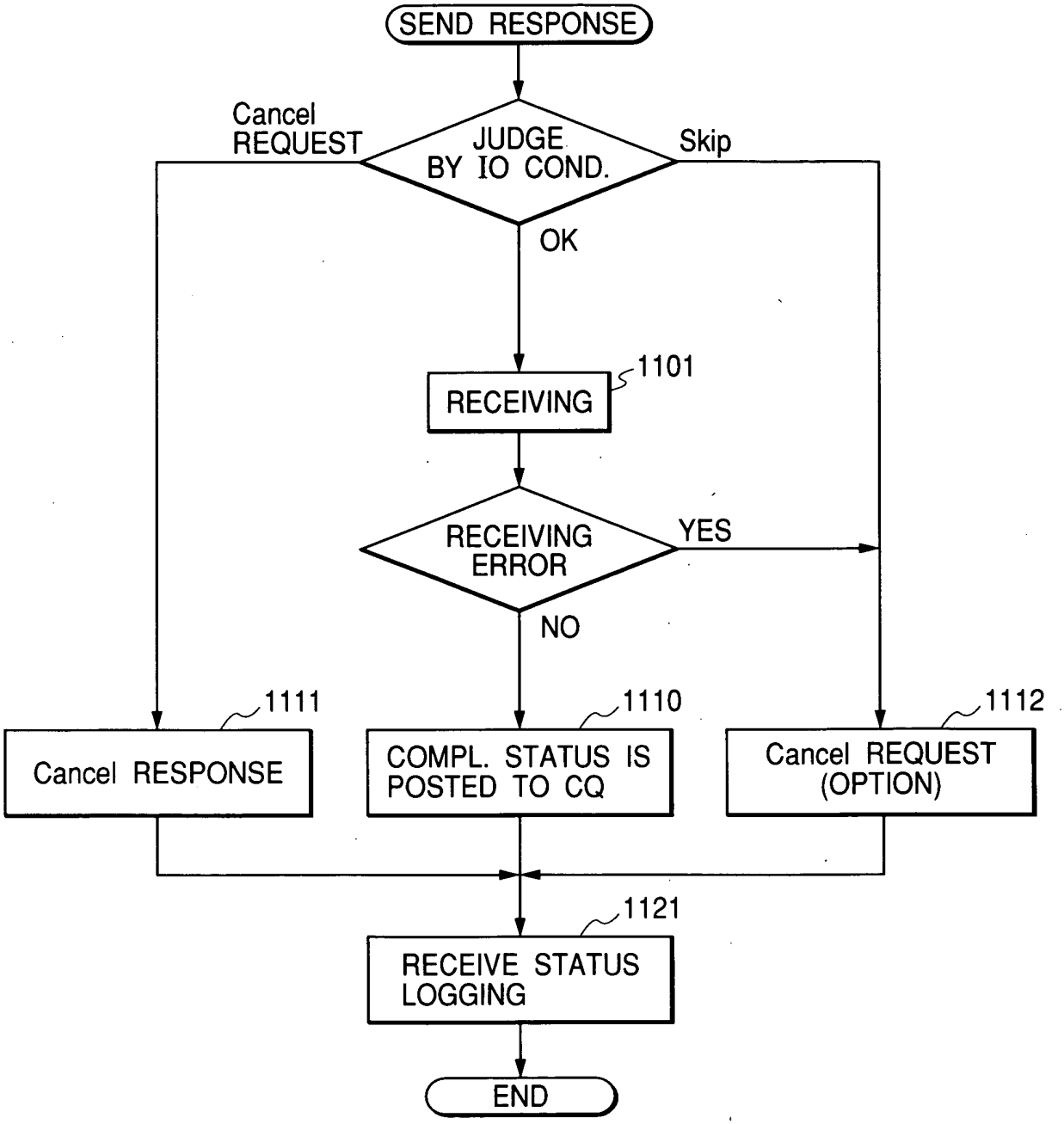

SEND RESPONSE
JUDGE BY IO COND.
Cancel REQUEST
Skip
OK
RECEIVING
1101
RECEIVING ERROR
YES
NO
Cancel RESPONSE
1111
COMPL. STATUS IS POSTED TO CQ
1110
Cancel REQUEST (OPTION)
1112
RECEIVE STATUS LOGGING
1121
END

FIG. 13

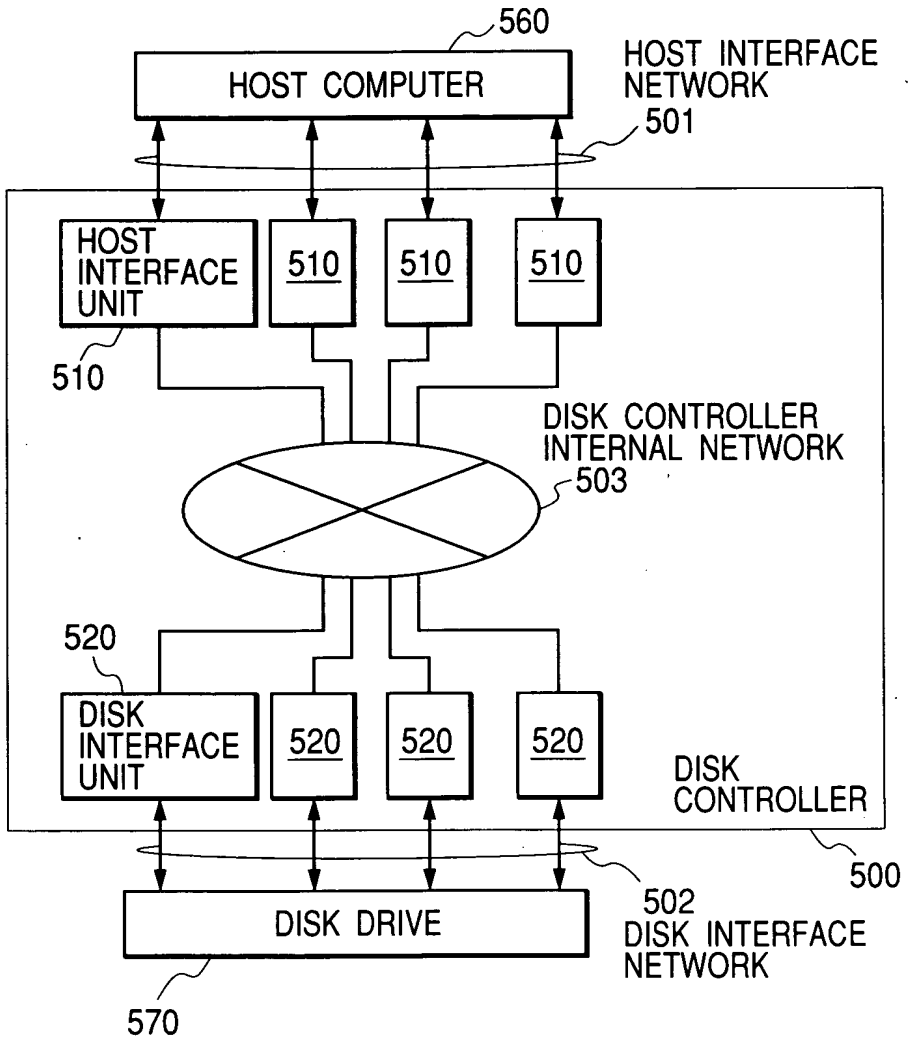

560
HOST COMPUTER
HOST INTERFACE NETWORK
501
HOST INTERFACE UNIT
510
510
510
510
DISK CONTROLLER INTERNAL NETWORK
503
520
DISK INTERFACE UNIT
520
520
520
DISK CONTROLLER
500
502
DISK INTERFACE NETWORK
DISK DRIVE
570

FIG. 14

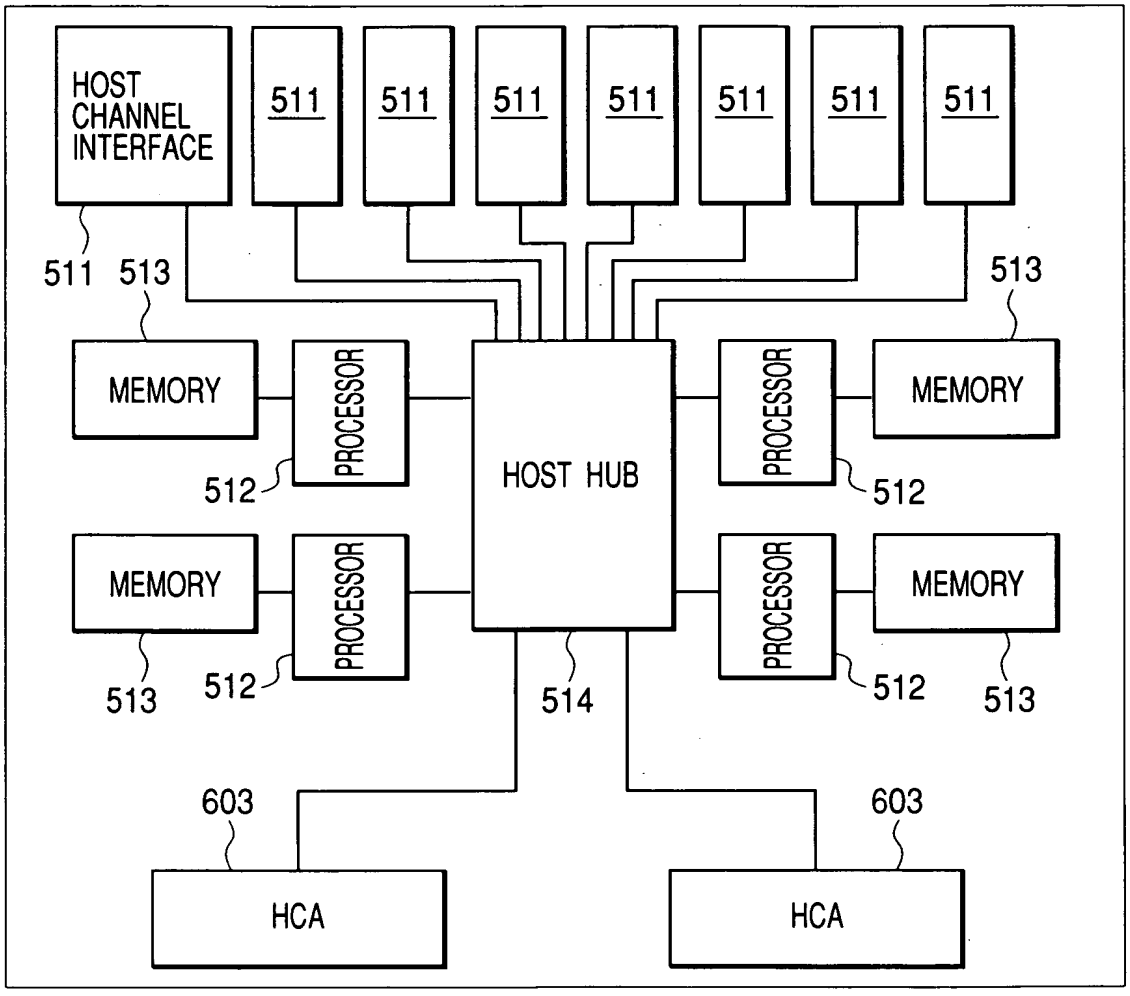

HOST CHANNEL INTERFACE
511
511
511
511
511
511
511
511
513
513
MEMORY
PROCESSOR
512
HOST HUB
PROCESSOR
MEMORY
512
MEMORY
PROCESSOR
513
512
514
PROCESSOR
MEMORY
512
513
603
603
HCA
HCA

FIG. 15

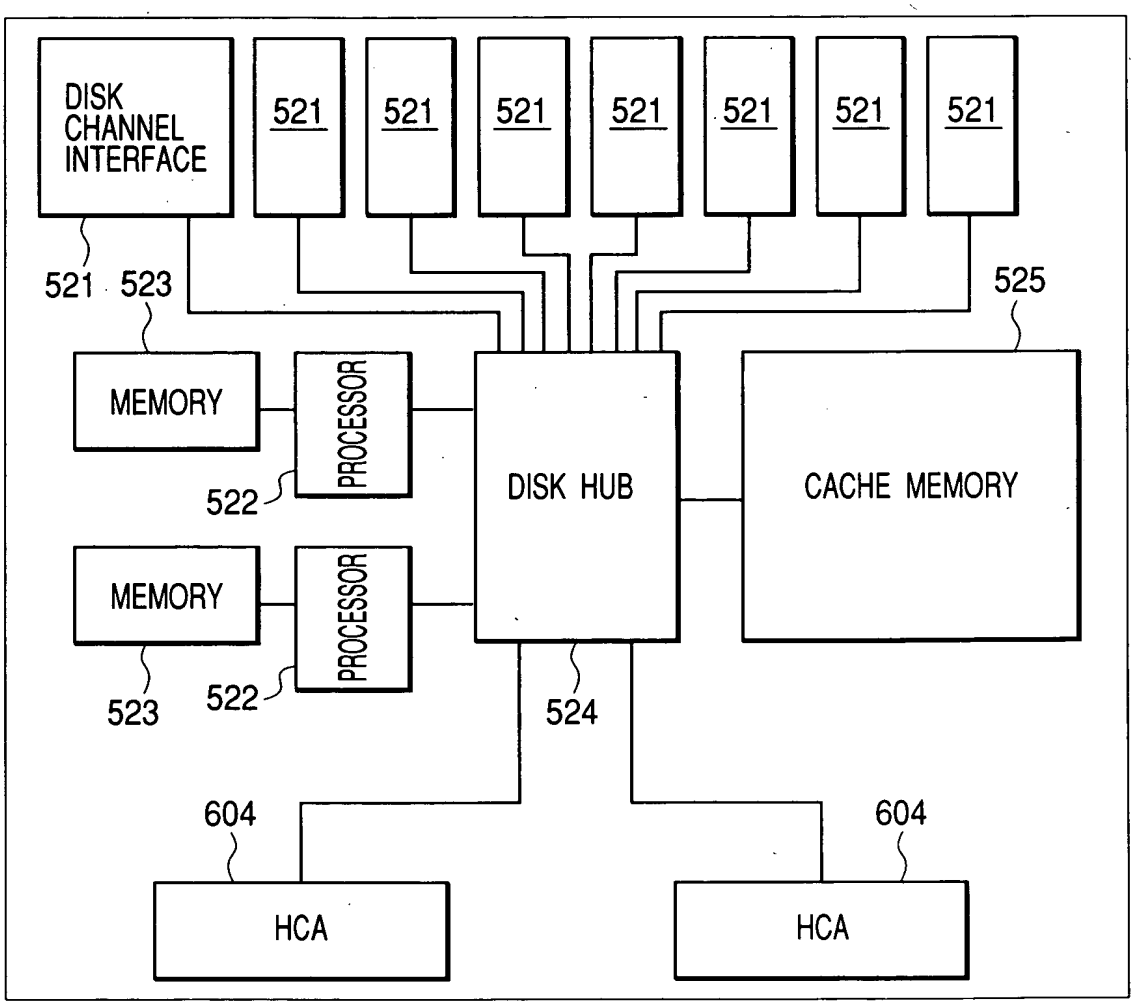

DISK CHANNEL INTERFACE
521
521
521
521
521
521
521
521
523
525
MEMORY
PROCESSOR
522
DISK HUB
CACHE MEMORY
MEMORY
PROCESSOR
523
522
524
604
604
HCA
HCA

FIG. 16

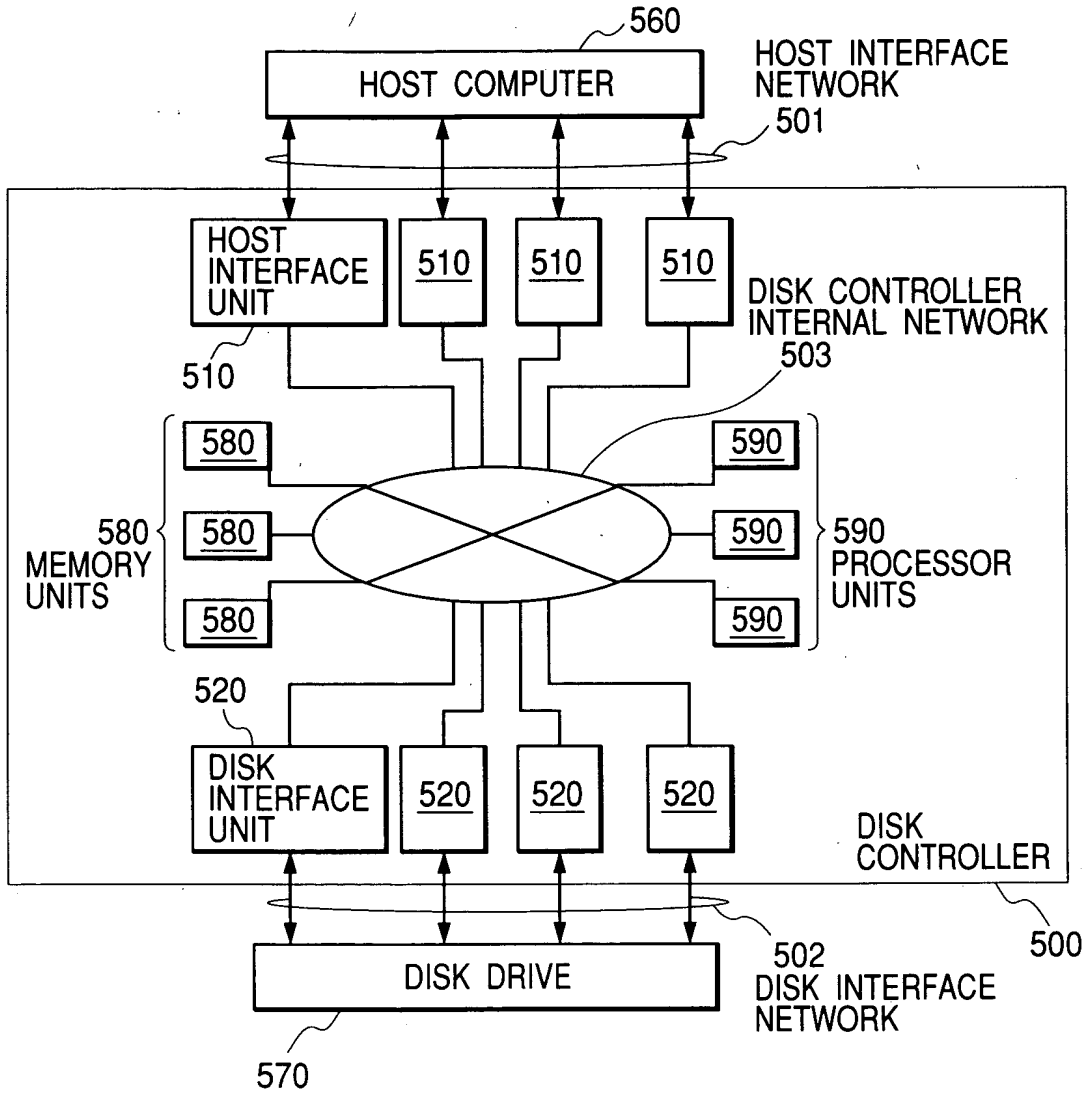

560
HOST COMPUTER
HOST INTERFACE NETWORK
501
HOST INTERFACE UNIT
510
510
510
510
DISK CONTROLLER INTERNAL NETWORK
503
580
580
580
580 MEMORY UNITS
590
590
590
590 PROCESSOR UNITS
520
DISK INTERFACE UNIT
520
520
520
DISK CONTROLLER
500
502
DISK INTERFACE NETWORK
DISK DRIVE
570

FIG. 17

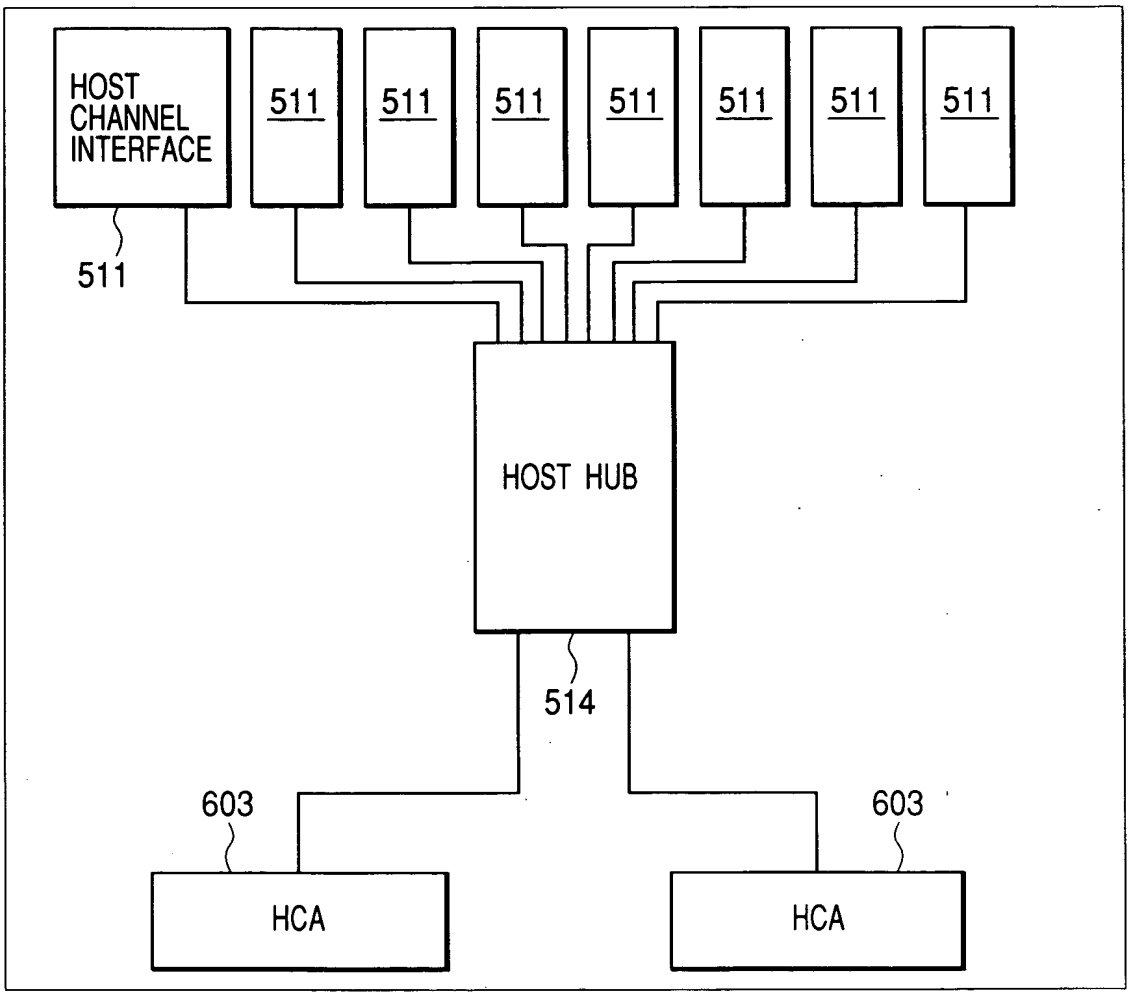
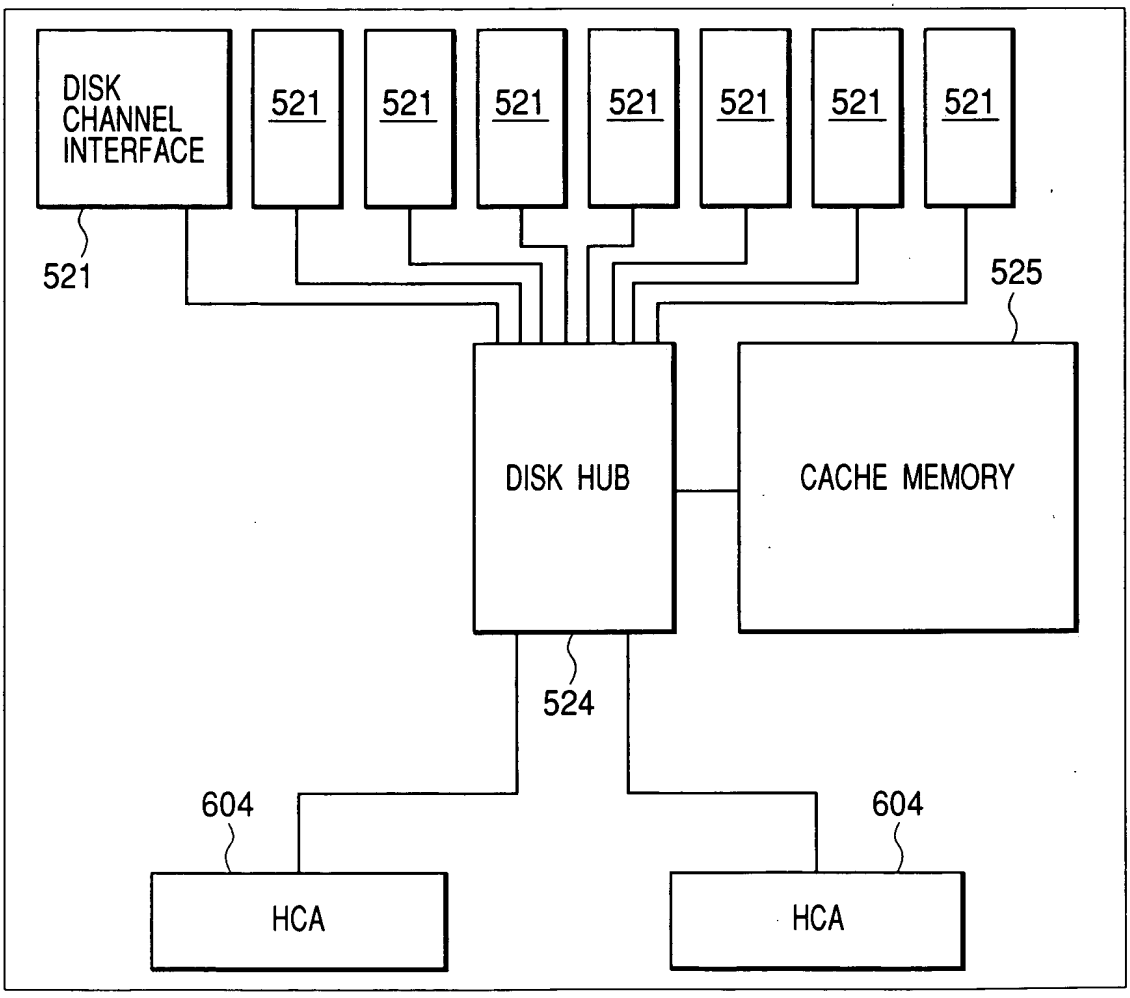

HOST CHANNEL INTERFACE
511
511
511
511
511
511
511
511
511
HOST HUB
514
603
603
HCA
HCA

FIG. 18


DISK CHANNEL INTERFACE
521
521
521
521
521
521
521
521
525
DISK HUB
CACHE MEMORY
524
604
604
HCA
HCA